Testing the Viability of 3D IC Thermal Side Channel Attack

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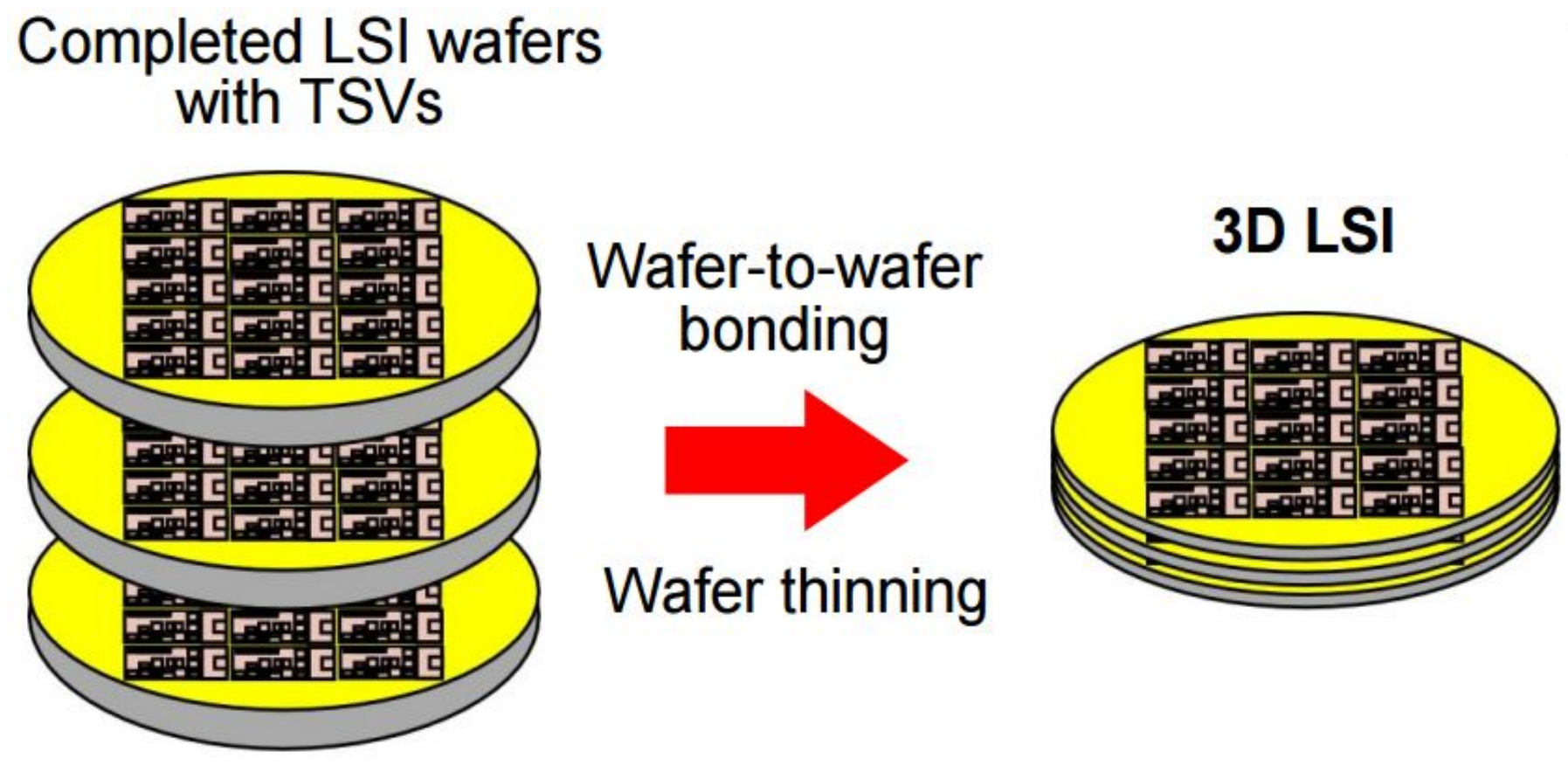
Motivation

- Active computer chips increase temperature.
- Smaller modern designs exacerbate this problem.
- This may allow Intellectual Property (IP) Pirates to collect data about design or programming because of temperature changes.

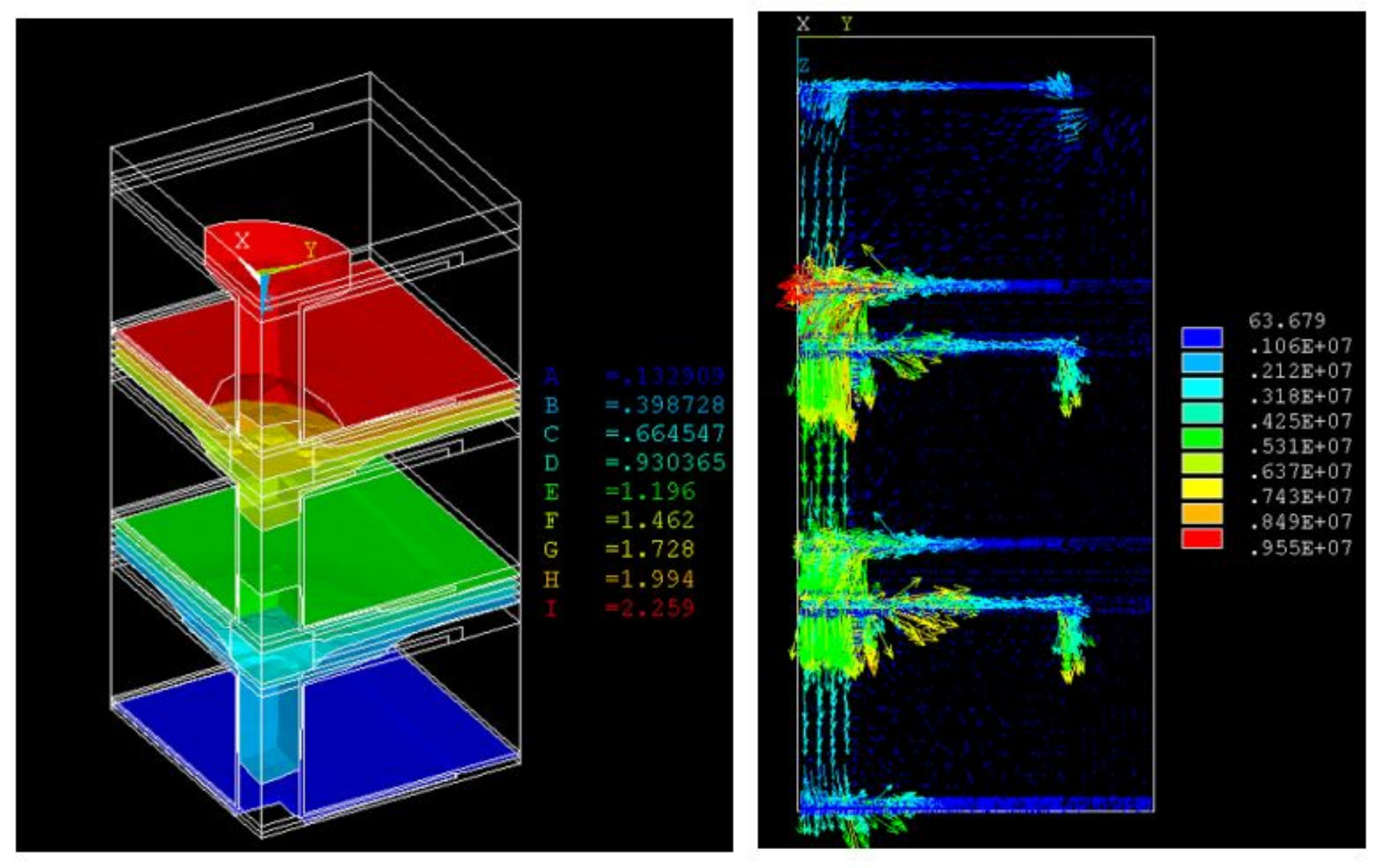
Background

3D ICs make use of circuit layouts connected in multiple directions.



-Fukushima et. al "Thermal issues of 3D ICs"

- To increase speed, IC components get smaller and closer together.
- Stacked components decrease interpose distance.
- Stacked components do not get more efficient.
- An increase in energy lost per unit volume increases total heat output.



Isothermal plane (°C)

Heat flux (W/m²)

-Fukushima et. al "Thermal issues of 3D ICs"

- Component proximity decreases heat dissipation.
- Temperature increases deeper in the chip.

Project Objective

To render flexible thermal models of components in 3D Integrated Circuits (ICs) and use those models to determine whether thermal features are consistent enough to allow analysis of chip design.

Methods

- Sapatnekar's Finite Element Method of thermal analysis is the backbone of this model.

$$[k_c] = \begin{bmatrix} +A & +B & +C & +D & +E & +F & +G & +H \\ +B & +A & +D & +C & +F & +E & +H & +G \\ +C & +D & +A & +B & +G & +H & +E & +F \\ +D & +C & +B & +A & +H & +G & +F & +E \\ +E & +F & +G & +H & +A & +B & +C & +D \\ +F & +E & +H & +G & +B & +A & +D & +C \\ +G & +H & +E & +F & +C & +D & +A & +B \\ +H & +G & +F & +E & +D & +C & +B & +A \end{bmatrix}$$

Output Temperature

$$[k_c]\{t\}=\{p\}$$

Input Power

$$\text{where } A = \frac{K_x hd}{9w} + \frac{K_y wd}{9h} + \frac{K_z wh}{9d},\ B = -\frac{K_x hd}{9w} + \frac{K_y wd}{18h} + \frac{K_z wh}{18d}$$

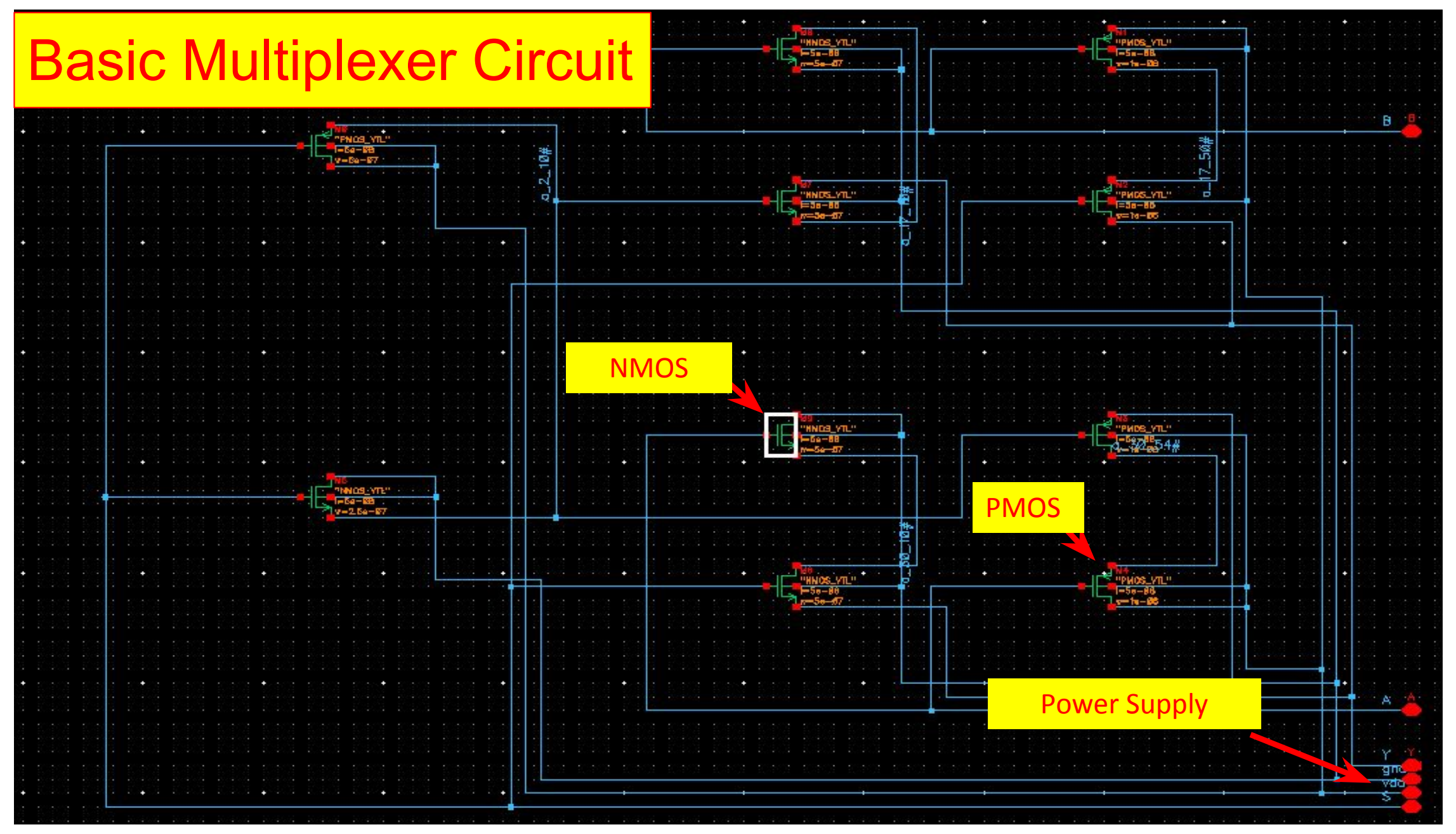
$$C = -\frac{K_x hd}{18w} - \frac{K_y wd}{18h} + \frac{K_z wh}{36d},\ D = \frac{K_x hd}{18w} - \frac{K_y wd}{9h} + \frac{K_z wh}{18d}$$

$$E = \frac{K_x hd}{18w} + \frac{K_y wd}{18h} - \frac{K_z wh}{9d},\ F = -\frac{K_x hd}{18w} + \frac{K_y wd}{36h} - \frac{K_z wh}{18d}$$

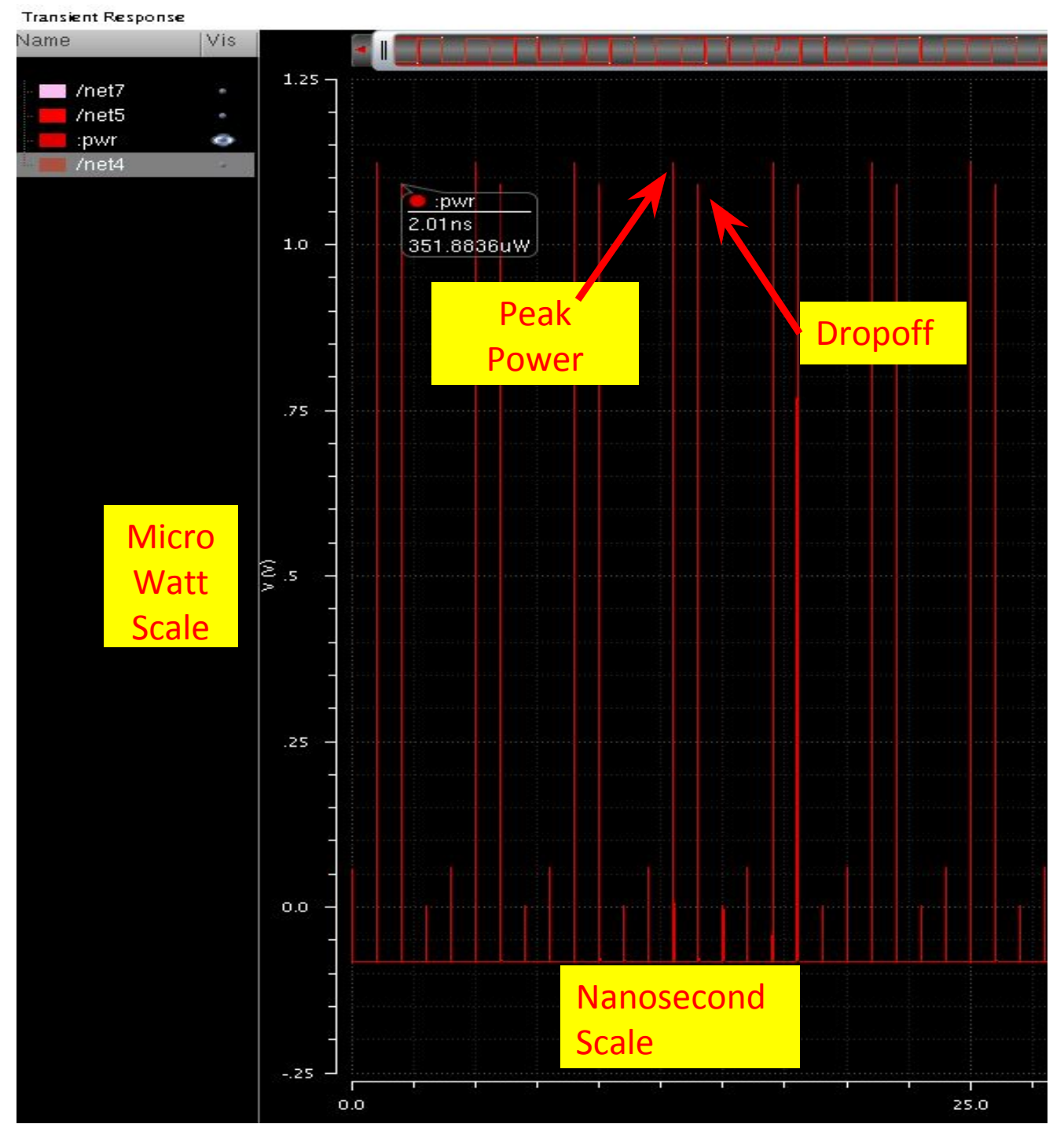
$$G = -\frac{K_x hd}{36w} - \frac{K_y wd}{36h} - \frac{K_z wh}{36d},\ H = \frac{K_x hd}{36w} - \frac{K_y wd}{18h} - \frac{K_z wh}{18d}$$

Here *w*, *h* and *d* represent height width and depth of the circuit housing. The *K* values represent the thermal dissipation values around the chip.

- Cadence Virtuoso was used to create viable circuit diagrams for a 3D chip environment.

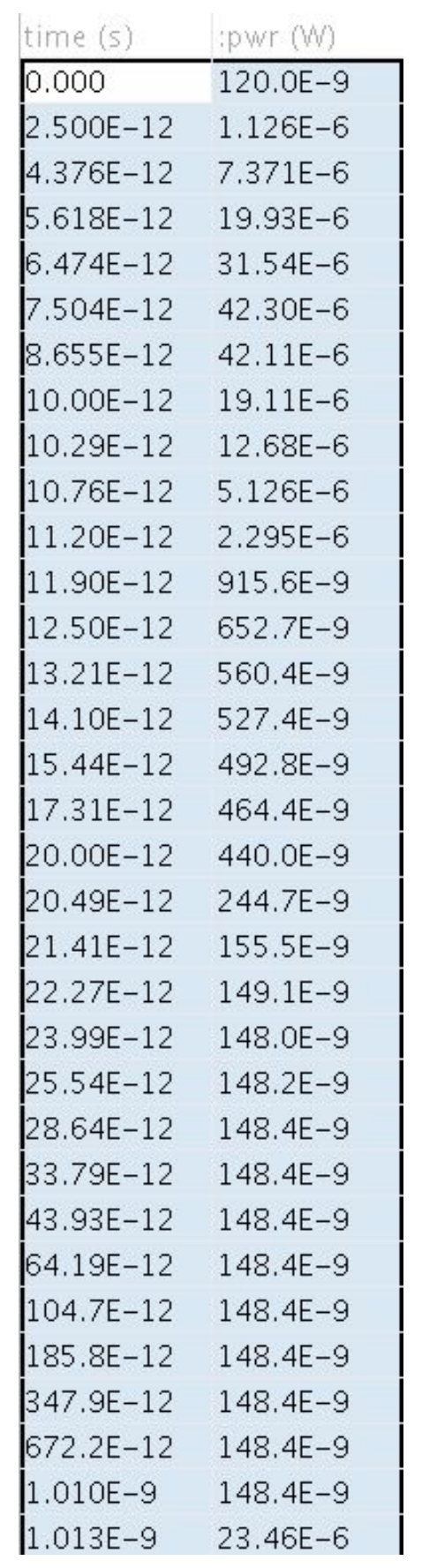


- This environment allows users to simulate circuits complete with voltage, current and *power loss*.



Example of power input and output in a simulated circuit.

The loss in power input to output bleeds out of the circuit as heat.

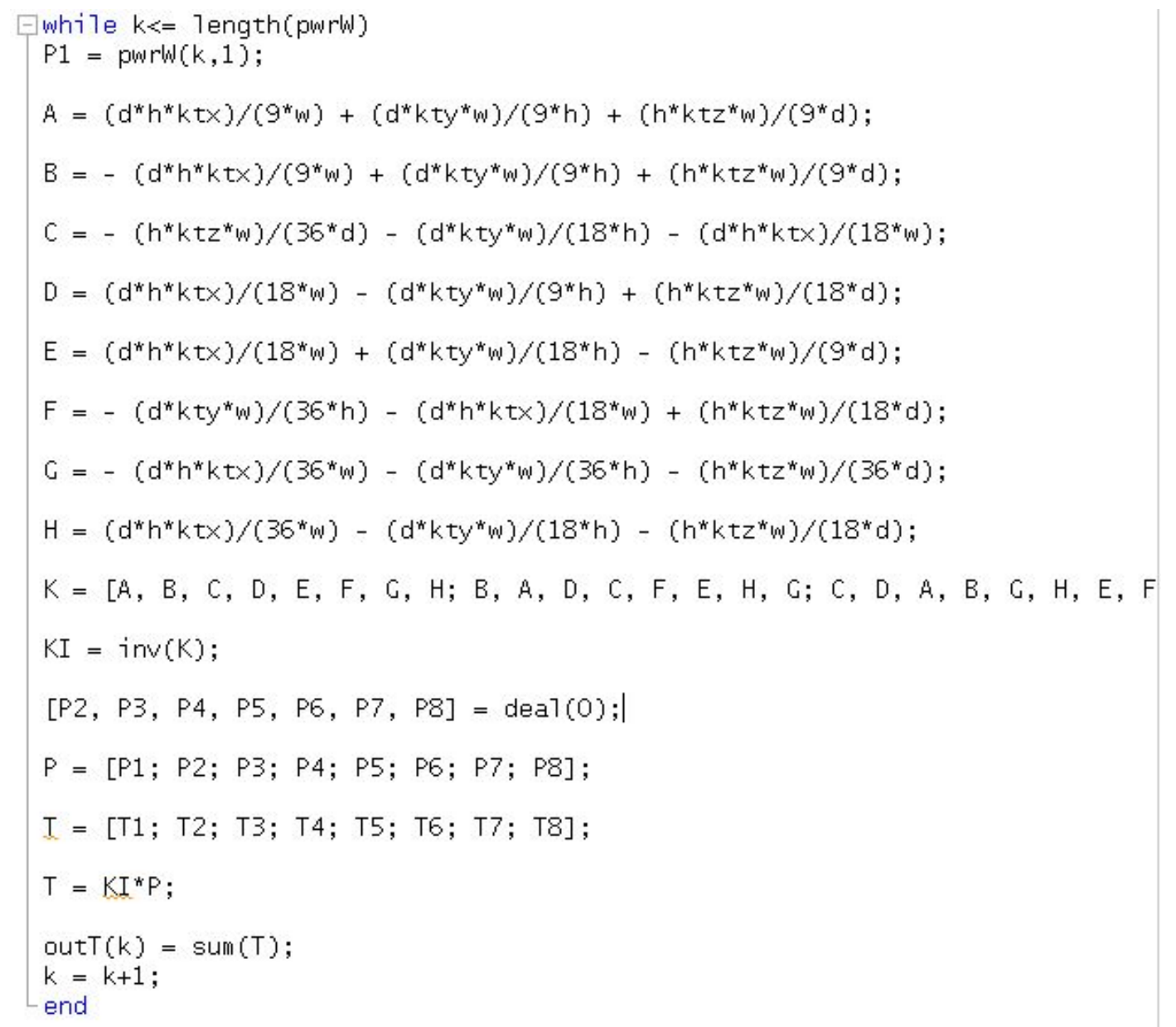


time (s)	:pwr (W)
0.000	120.0E-9
2.500E-12	1.126E-6
4.376E-12	7.371E-6
5.618E-12	19.93E-6
6.474E-12	31.54E-6
7.504E-12	42.30E-6
8.655E-12	42.11E-6
10.00E-12	19.11E-6
10.29E-12	12.68E-6
10.76E-12	5.126E-6
11.20E-12	2.295E-6
11.90E-12	915.6E-9
12.50E-12	652.7E-9
13.21E-12	560.4E-9
14.10E-12	527.4E-9
15.44E-12	492.8E-9
17.31E-12	464.4E-9
20.00E-12	440.0E-9
20.49E-12	244.7E-9
21.41E-12	155.5E-9
22.27E-12	149.1E-9
23.99E-12	148.0E-9
25.54E-12	148.2E-9
28.64E-12	148.4E-9
33.79E-12	148.4E-9
43.93E-12	148.4E-9
64.19E-12	148.4E-9
104.7E-12	148.4E-9
185.8E-12	148.4E-9
347.9E-12	148.4E-9
672.2E-12	148.4E-9
1.010E-9	148.4E-9
1.013E-9	23.46E-6

- A matrix of power values from Virtuoso can be imported into a MATLAB program.
- MATLAB is well suited to building functional relationships between matrices and arrays.
- The program can extract data from a .csv.
- It can plot individual temperature values or averages.
- The program also allows for changes in chip size as well as variation of material around the circuit.

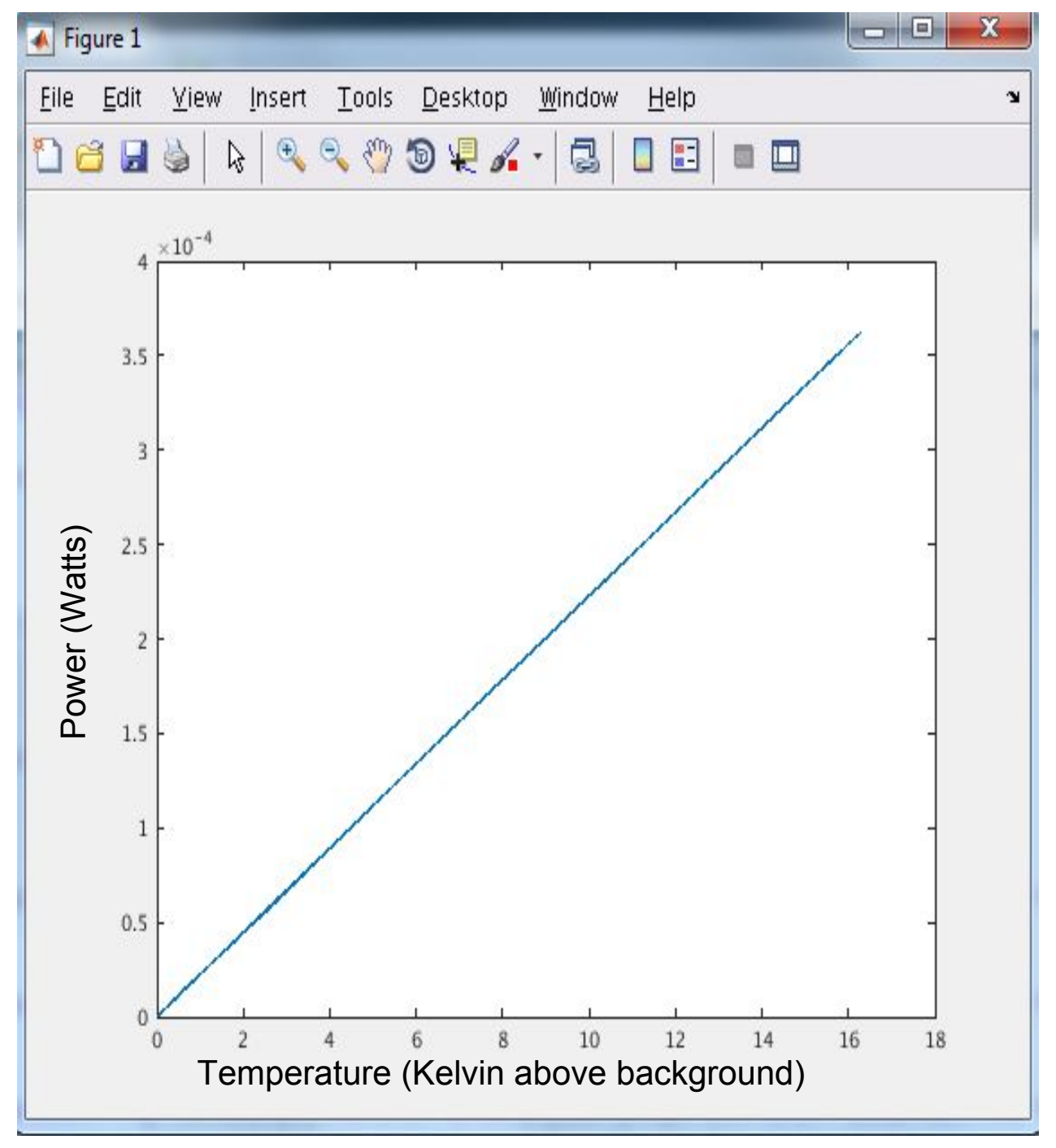
Example code showing the components of the matrix in array form.

MATLAB allows for iterative testing.



```
while k<= length(pwrW)
P1 = pwrW(k,1);

A = (d*h*ktx)/(9*w) + (d*kty*w)/(9*h) + (h*ktz*w)/(9*d);

B = - (d*h*ktx)/(9*w) + (d*kty*w)/(9*h) + (h*ktz*w)/(9*d);

C = - (h*ktz*w)/(36*d) - (d*kty*w)/(18*h) - (d*h*ktx)/(18*w);

D = (d*h*ktx)/(18*w) - (d*kty*w)/(9*h) + (h*ktz*w)/(18*d);

E = (d*h*ktx)/(18*w) + (d*kty*w)/(18*h) - (h*ktz*w)/(9*d);

F = - (d*kty*w)/(36*h) - (d*h*ktx)/(18*w) + (h*ktz*w)/(18*d);

G = - (d*h*ktx)/(36*w) - (d*kty*w)/(36*h) - (h*ktz*w)/(36*d);

H = (d*h*ktx)/(36*w) - (d*kty*w)/(18*h) - (h*ktz*w)/(18*d);

K = [A, B, C, D, E, F, G, H; B, A, D, C, F, E, H, G; C, D, A, B, G, H, E, F

KI = inv(K);

[P2, P3, P4, P5, P6, P7, P8] = deal(0);

P = [P1; P2; P3; P4; P5; P6; P7; P8];

T = [T1; T2; T3; T4; T5; T6; T7; T8];

T = KI*P;

outT(k) = sum(T);
k = k+1;
end
```

Results



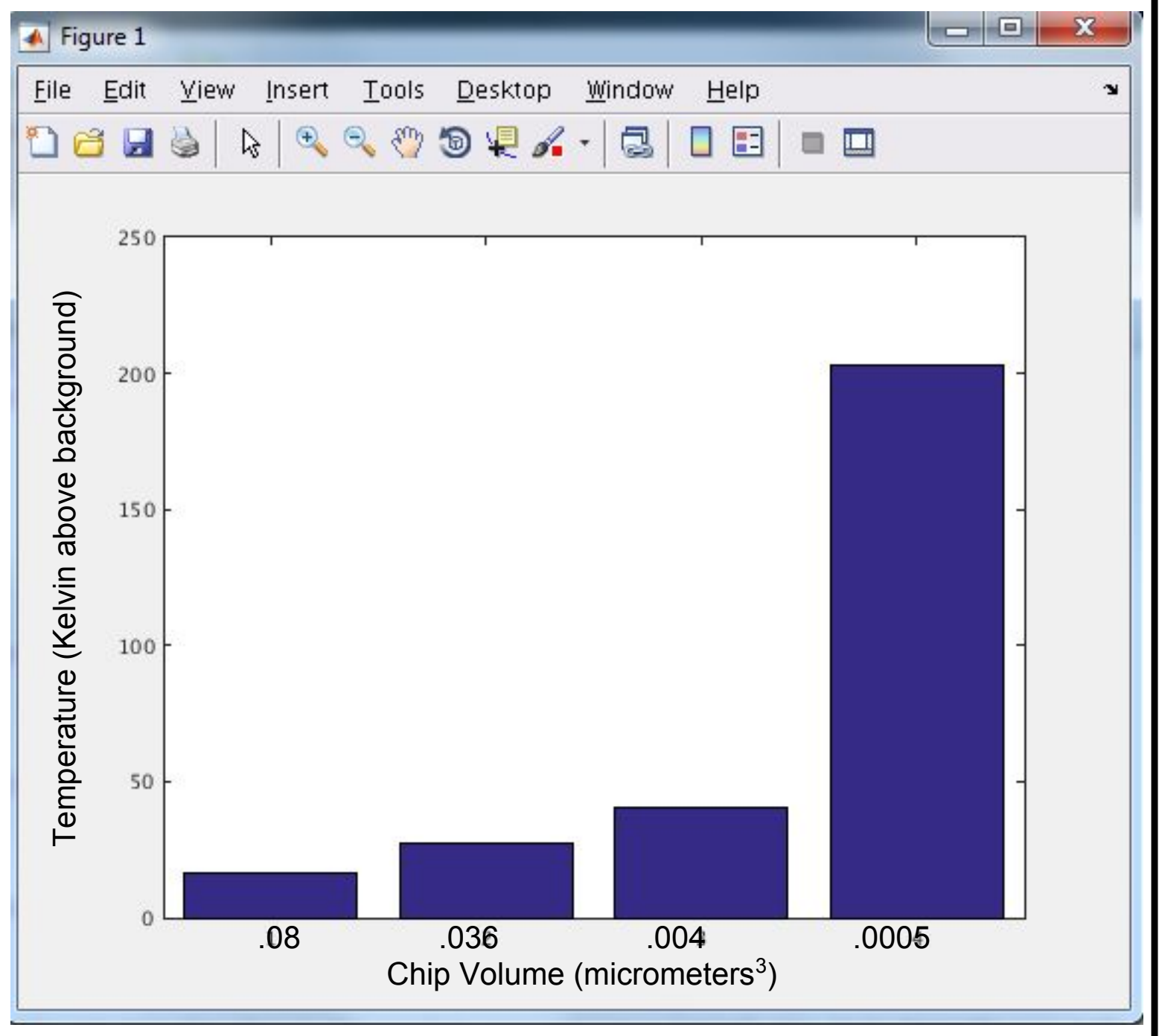
The model behaved as predicted. Increases in power led to increases in temperature gradient.

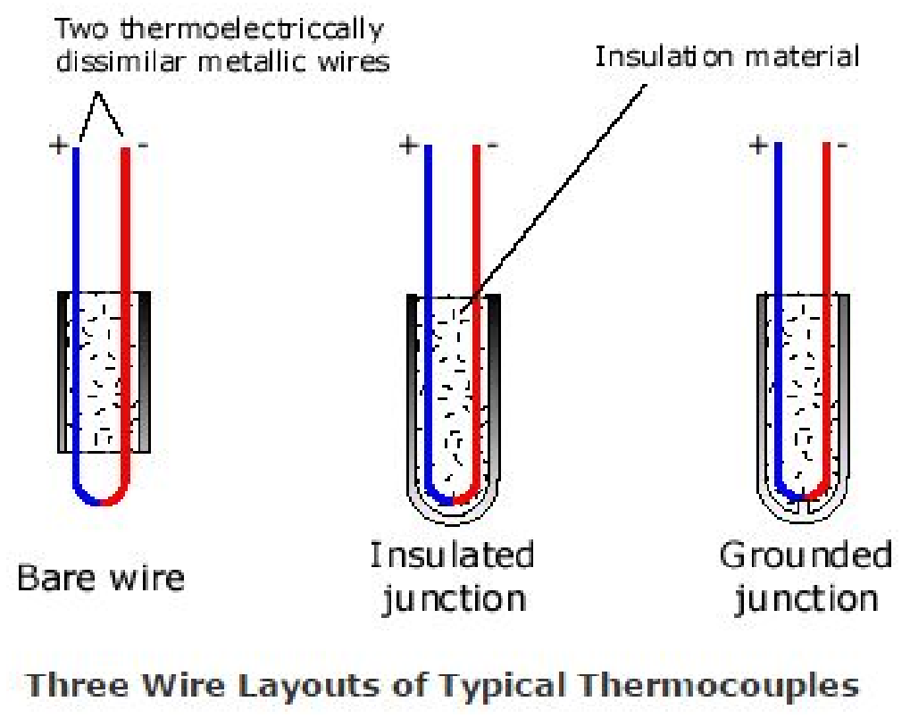
The example used thousands of power values.

- Temperature changes can be extreme, with a microwatt power change producing a 4° shift.
- The model allows for comparisons of circuit temperatures when the chip environment gets larger or smaller, or the materials around it change their thermal conductivity.

In this example, thermal gradient is compared to chip volume.

As chip scale gets smaller, average temperature gets much higher, compared to background.



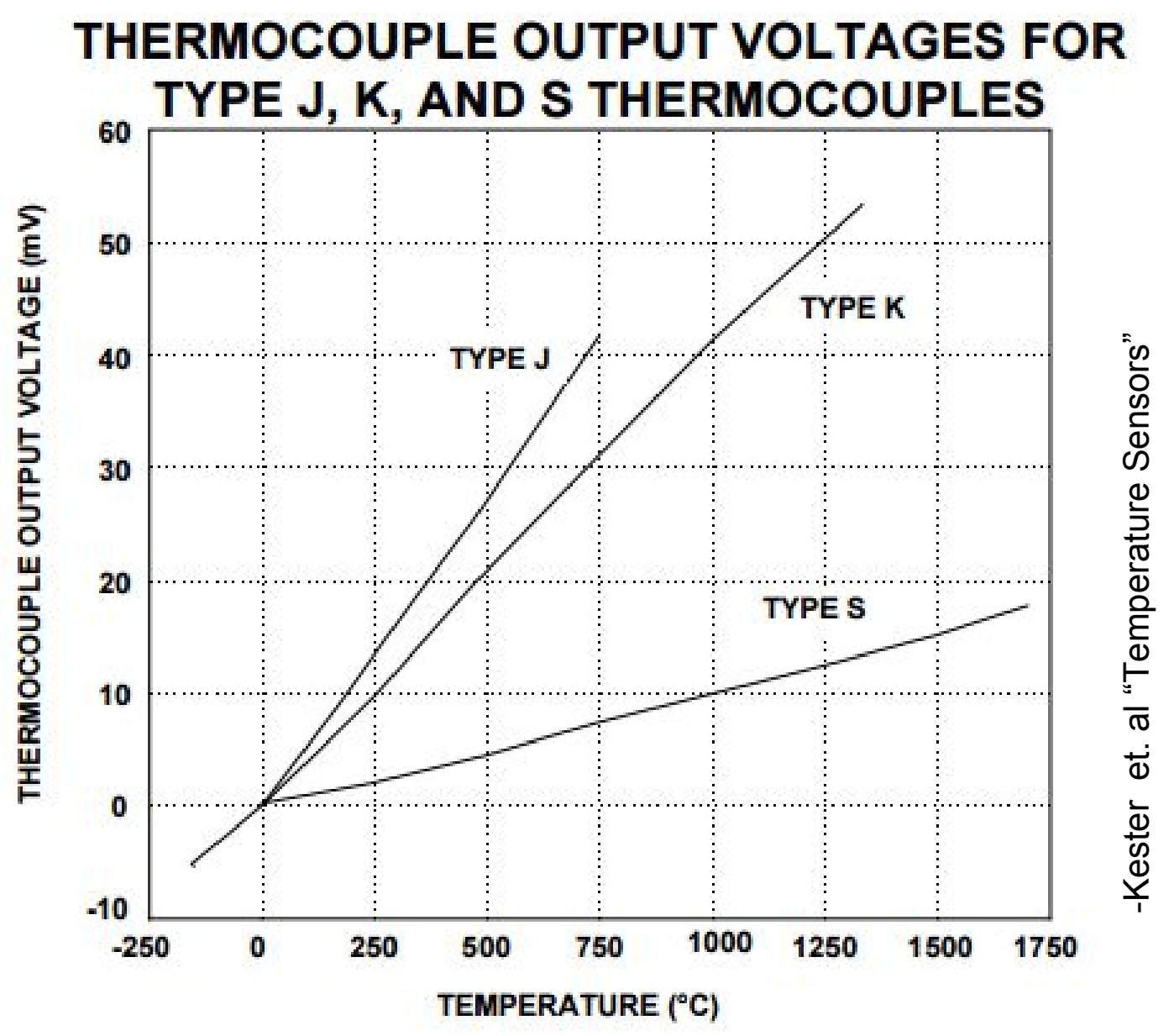


Three Wire Layouts of Typical Thermocouples

-Kester et. al "Temperature Sensors"

- Modern thermocouples make use of two wires with different resistance to determine temperature variance.
- Thermocouples work on the principle that the warmer a wire gets, the slower current flows through it.

- A 25° change in local temperature can change the voltage of a thermocouple by 1 mV.
- This could simultaneously make the circuit less efficient as it increases thermal loading.



-Kester et. al "Temperature Sensors"

Conclusions

- With small modifications, it is possible that a simple thermocouple could determine not only when 1 particular component is activated, but when it is deactivated.
- The geometric increase in thermal output as circuits get smaller means that a millivolt difference may cause a measurable temperature change in a component.

References

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