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CASPER Toolflow Based FPGA Design for Lightning Radio Interferometers

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Abstract

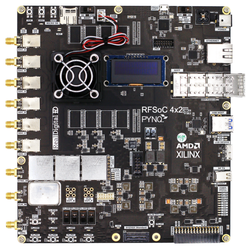
Broadband radio interferometers have enabled many recent discoveries in the lightning field. As the field pushes to resolve faster lightning processes on smaller spatial scales, it demands next generation lightning interferometers to run on higher sampling rates and to support more radio channels. In addition, flexibility in the operation configuration of the instrument is highly desirable because of the broad emission spectrum and wide magnitude of lightning's subprocesses. Within a modest budget, Xilinx' RFSoC boards offer a potential solution, but this often requires the development of custom FPGA designs, which is known to be difficult.

CASPER Toolflow is a collection of FPGA digital signal processing utilities and programming tools developed for radio astronomy. It supports several of the latest RFSoC boards with multiple (e.g., 16) ADCs, each capable of multi-gigahertz sampling rates. The captured data can be transferred out of FPGA via 100 GbE connections. In this talk, we will present our effort to utilize the CASPER Toolflow to develop a FPGA design for RIFTS (Radio Interferometer for Thunderstorm Studies) and share our experiences working with the RFSoC ZCU 216 board. Our design methodology, developed functional blocks, and hardware testing practices can be readily adapted for other CASPER Toolflow supported boards. We will present the capture results of multiple (e.g., 8) radio channels with a rate of giga-samples per second each and discuss how the data is processed in the subsequent digital signal processing pipeline and then transferred to external storage devices.

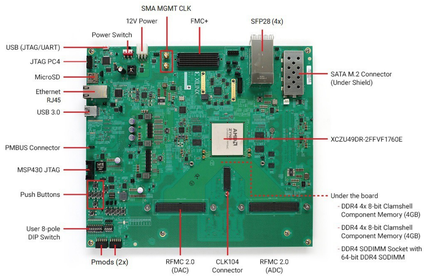
Introduction

An affordable solution for developing the next generation lightning interferometer is provided by the Xilinx RFSoC boards, which integrate high-speed RF ADCs/DACs with FPGA. The main features of the RFSoC include:

- Direct RF sampling
- Multiple RF channels, each capable of supporting gigasamples per second (GSPS) data rate
- Gigabytes of DDR4 memory
- 100 GbE Ethernet interface

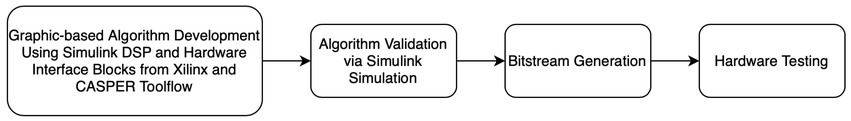


RFSoC 4x2 Board (5 GSPS)



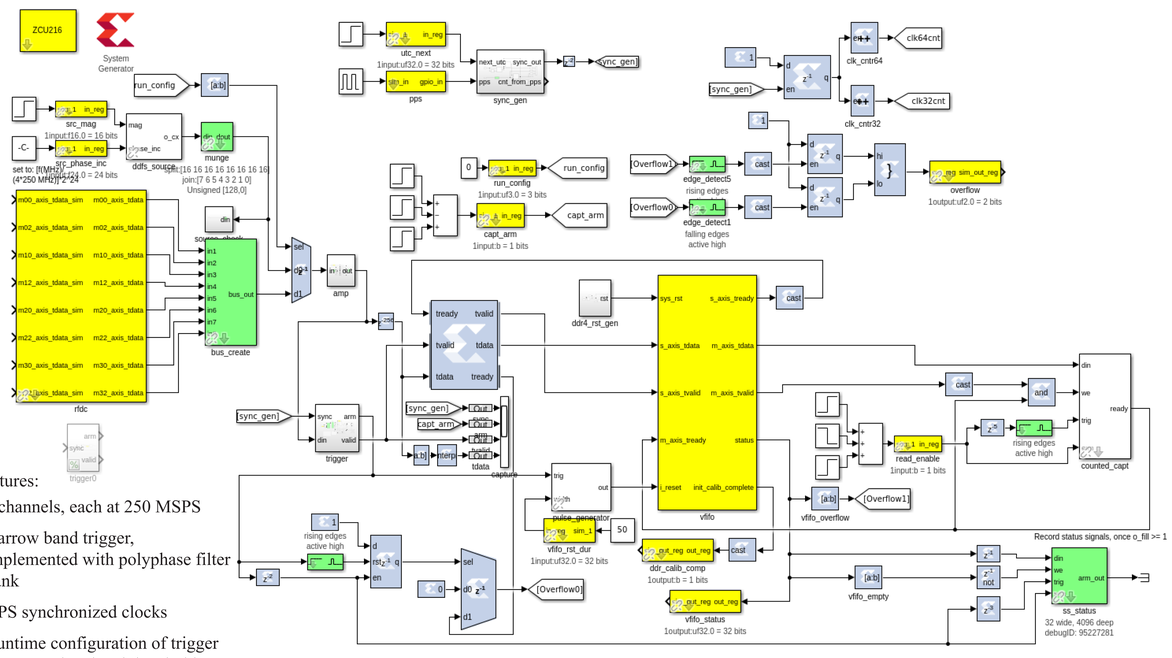
ZCU 216 Board (2.5 GSPS)

This, however, requires the development of custom FPGA designs, which is known to be challenging. A relatively accessible option is to use Matlab/Simulink and CASPER Toolflow (Collaboration for Astronomical Signal Processing and Electronics Research). The CASPER Toolflow is a collection of toolsets developed for designing and implementing high-performance digital signal processing (DSP) systems, allowing for rapid prototyping and deployment of DSP algorithms. A typical workflow for creating a FPGA design using the CASPER Toolflow is as follows:



In this approach, the access to hardware components (e.g., ADCs/DACs, bram, software registers) is provided by the hardware interface blocks from the CASPER Toolflow, known as "yellow blocks." The Toolflow invokes Xilinx tools to compile the Simulink design and generate bitstream code. A Python library, casperfpga, is used to interact and interface with the hardware, including firmware reconfiguration and reading/writing bram and registers.

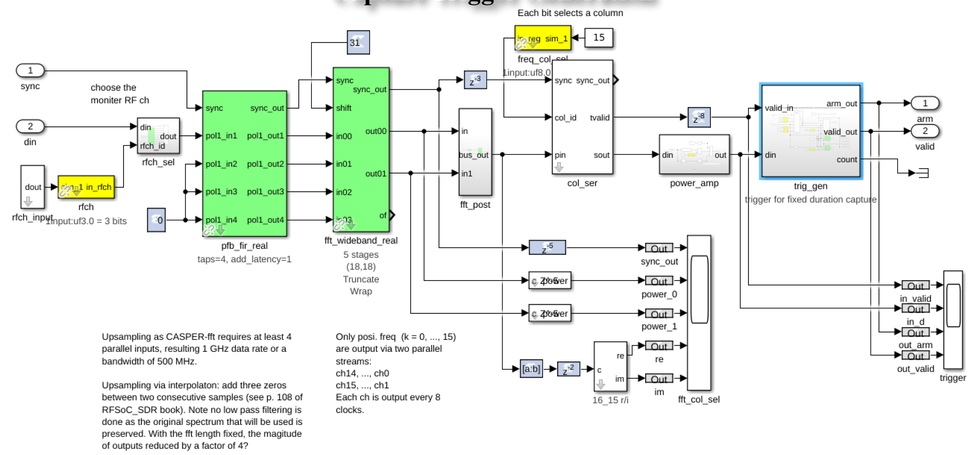
An Example Design



Main features:

- 8 channels, each at 250 MSPS
- Narrow band trigger, implemented with polyphase filter bank
- GPS synchronized clocks
- Runtime configuration of trigger frequency band and threshold

Capture Trigger Generation

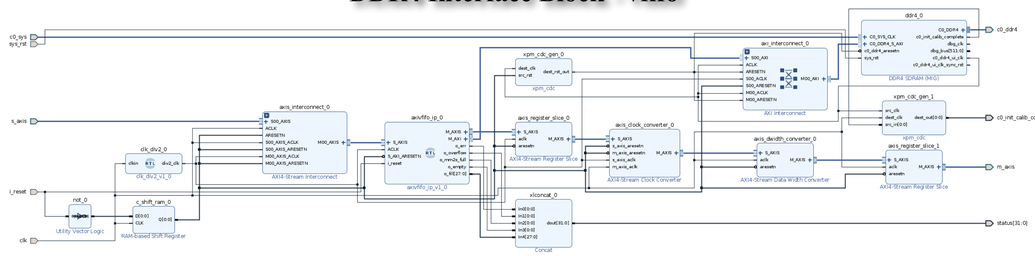


Upsampling as CASPER-fft requires at least 4 parallel inputs, resulting 1 GHz data rate or a bandwidth of 500 MHz.

Upsampling via interpolaton: add three zeros between two consecutive samples (see p. 108 of RFSoC_SDR book). Note no low pass filtering is done as the original spectrum that will be used is preserved. With the fft length fixed, the magitude of outputs reduced by a factor of 4?

Only posi. freq (k = 0, ..., 15) are output via two parallel streams:
ch14, ..., ch0
ch15, ..., ch1
Each ch is output every 8 clocks.

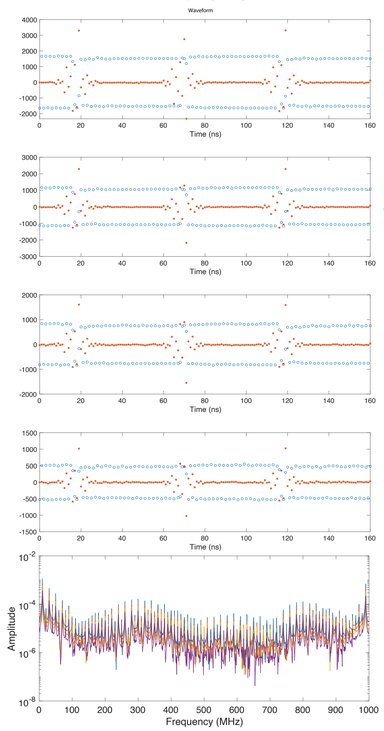
DDR4 Interface Block - vfifo



Test Results

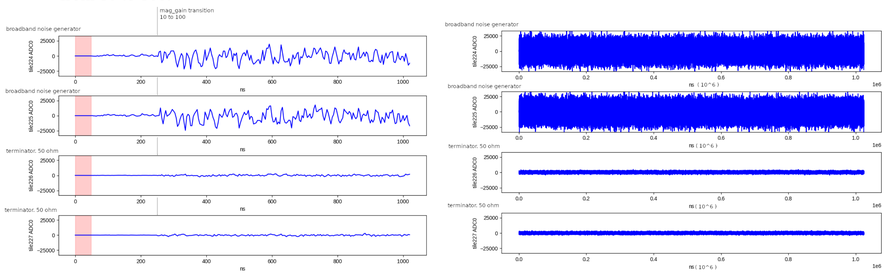
Multiple Channel Capture Test

The 10 MHz reference clocks distributed by a GPS system were connected to the inputs of 4 RF channels with varying degrees of attenuation.



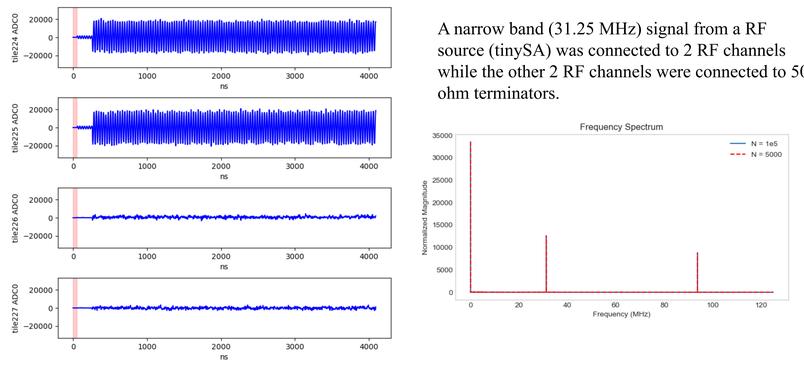
Trigger Test

The signal from a broadband noise generator was split and then injected into 2 RF channels while the other 2 RF channels were connected to 50 ohm terminators. The triggering was simulated as a sudden increase of digital gain from 10 to 100.



RF Signal Recording Test

A narrow band (31.25 MHz) signal from a RF source (tinySA) was connected to 2 RF channels while the other 2 RF channels were connected to 50 ohm terminators.



Summary

We have investigated the methodology of designing FPGA systems using the CASPER Toolflow. Developing an FPGA design involves a complex workflow consisting of various stages and often requires multiple design iterations. The CASPER Toolflow provides a relatively accessible workflow for lightning researchers to leverage CASPER-supported FPGA boards. The Simulink blocksets offered by the CASPER Toolflow allow developers to access critical hardware resources (e.g., ADCs/DACs, bram, software registers) and DSP algorithms (e.g., FFT, polyphase filter banks) without requiring detailed knowledge of the underlying hardware components.

However, the current version of the CASPER Toolflow lacks support for DDR memory. Access to DDR memory on FPGA boards is crucial for high-performance lightning instrumentation. To address this, developers may need to create a CASPER-style Simulink block to integrate DDR memory. This process can be both challenging and time-consuming.

References

CASPER Toolflow: https://casper-toolflow.readthedocs.io/en/latest/index.html

Acknowledgments

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